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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,964	09/09/2003	Sriram Satakopan	004-8841	4133

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ZAGORIN O'BRIEN GRAHAM LLP
7600B N. CAPITAL OF TEXAS HWY.
SUITE 350
AUSTIN, TX 78731

EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/657,964	SATAKOPAN ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/10/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1- 23 are rejected under 35 U.S.C. 102(e) as being unpatentable by Chen (US Patent 6,687,888).

2. As to claims 1, 15, 18, 20 and 23 Chen discloses:

(1) A method for use in connection with an integrated circuit design, the method comprising:

selecting a subset of low threshold voltage variants (Reduced-VT/fast-but-leaky devices (gates)) of gate instances for substitution with respective standard threshold voltage variants (normal/standard-VT/slow-but not-leaky devices (gates)) thereof (Abstract; col.5, ll.40-48; col.7, ll.9-18; col.8, ll.39-46);

(15) A semiconductor integrated circuit comprising:

a plurality of gate instances (col.7, ll.19-30; col.8, ll.39-46);

circuit paths defined through respective ones of the gate instances (col.8, ll.30-54);

wherein a subset of the gate instances are standard threshold voltage variants substituted in the semiconductor integrated circuit based on a measurement (calculating) indicating a low threshold voltage variant penalty for the circuit paths including the subset of the gate instances (Abstract; col.5, ll.40-48; col.7, ll.9-18; col.8, ll.39-46; col.8, ll.47-54);

(18) A computer readable encoding of a semiconductor integrated circuit design, the computer readable encoding comprising (col.13, ll.20-25):

one or more design file media encoding representations of a plurality of gate instances (col.3, ll.49-67; col.7, ll.19-30; col.8, ll.39-46); and

one or more design file media encoding representations of circuit paths defined through respective ones of the gate instances (col.3, ll.49-67; col.7, ll.19-30; col.8, ll.30-54);

wherein a subset of the gate instances are standard threshold voltage variants substituted in the semiconductor integrated circuit based on a measurement (calculating) indicating a low threshold voltage variant timing penalty (Abstract; col.5, ll.40-48; col.7, ll.9-18; col.8, ll.39-46; col.8, ll.47-54);

(20) A method of making a computer readable media product that encodes a design file representation of a semiconductor integrated circuit, the method comprising (col.13, ll.20-25):

preparing the one or more design files for the semiconductor integrated circuit including at least one low threshold voltage instance and performing timing analysis thereon (col.3, ll.49-67; col.7, ll.19-30; col.8, ll.30-54);

substituting at least one of the low threshold voltage instances of the semiconductor integrated circuit with a standard threshold voltage instance (Abstract; col.5, ll.40-48; col.7, ll.9-18; col.8, ll.39-46); and

generating one or more design file outputs that encode representations of the semiconductor integrated circuit, including the substituted standard threshold voltage instances (col.4, ll.1-9; col.6, ll.14-27; col.7, ll.41-52); and

supplying the one or more design tile outputs as at least part of the computer readable media product (col.13, ll.20-25);

(23) An apparatus (computer) comprising:

means for processing one or more design files for a semiconductor integrated circuit, the one or more design files encoding representations of a plurality of gate instances and circuit paths (col.3, ll.49-67; col.7, ll.19-30; col.8, ll.30-54);

means for selecting at least one of the gate instances based on a measurement that indicates a low threshold voltage variant timing penalty (Abstract; col.5, ll.40-48; col.7, ll.9-18; col.8, ll.39-46); and

means for substituting at least one of the low threshold voltage gate instance representations with respective standard threshold voltage variants thereof (col.5, ll.40-48; col.7, ll.9-18; col.8, ll.39-46).

3. As to claims 2-14, 16-17, 19 and 21-22 Chen recites:

(2), (21) The method, wherein the selecting is based at least in part on a measurement indicating a substantial low threshold voltage variant timing penalty (col.8, ll.48-54);

(3), (4), (16), (17), (19), (22) The method/circuit/program, wherein the measurement includes an input slew rate of each gate instance (rise and fall times expected on the inputs of the gate) in a circuit path, wherein the input slew rate is based in part on falling edge input transitions (col.10, ll.50-51);

(5) The method of claim 2, wherein the measurement includes a delay for a low threshold voltage (col.7, ll.31-51; col.12, ll.65-67; col.13, ll.1-19);

(6)-(10) The method, wherein the measurement includes a first maximum delay timing path calculation for a circuit path including a low threshold voltage variant and a second maximum delay timing path calculation including a standard threshold voltage variant corresponding to the low threshold voltage variant, and calculating the difference between the first and second maximum delay timing path calculation (col.12, ll.65-67; col.13, ll.1-19);

(11) The method of claim 2, wherein the timing penalty exceeds a threshold (col.8, ll.48-54);

(12) The method of claim 1, further comprising substituting in the integrated circuit design, the selected low threshold voltage variants with the respective standard threshold voltage variants thereof (Abstract; col.5, ll.40-48; col.7, ll.9-18; col.8, ll.39-46);

(13) The method of claim 12, further comprising fabricating an integrated circuit including the substituted standard threshold voltage gate instances (col.4, ll.1-9; col.6, ll.14-27; col.7, ll.41-51);

(14) The method of claim 1, further comprising preparing the integrated circuit design and thereafter performing the selecting for substitution (Abstract; col.5, ll.40-48; col.7, ll.9-18; col.8, ll.39-46).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Naum Levin

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Naum Levin

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